



# UNITED STATES PATENT AND TRADEMARK OFFICE

mf

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/623,283

07/18/2003

Cory Watkins

A126.111.102

2405

25281

7590

09/12/2006

DICKE, BILLIG & CZAJA, P.L.L.C.  
FIFTH STREET TOWERS  
100 SOUTH FIFTH STREET, SUITE 2250  
MINNEAPOLIS, MN 55402

EXAMINER

LE, BRIAN Q

ART UNIT

PAPER NUMBER

2624

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/623,283

Applicant(s)

WATKINS, CORY

Examiner

Brian Q. Le

Art Unit

2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/18/2003</u> . | 6) <input type="checkbox"/> Other: ____.  |

## ***Double Patenting***

### **Nonstatutory Double Patenting**

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-7 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7 respectively of copending Application No. 10/623,282. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

- While each of the limitations of the instant claims is exactly recited in the copending claims, the copending claims include additional recitation of “and columns”.

Art Unit: 2624

- Because the instant claims use the transitional term “including”, they fail to preclude the additional limitations of the copending Application claims. Furthermore, each limitation of the instant claims is stipulated by the copending Application claims, so that the instant claims are anticipated by copending Application claim, and therefore are obvious in view of the copending Application. (Anticipation is “the ultimate or epitome of obviousness” (*In re Kalm*, 154 USPQ 10 (CCPA 1967), also *In re Dailey*, 178 USPQ 293 (CCPA 1973) and *In re Pearson*, 181 USPQ 641 (CCPA 1974)). Because instant claims are anticipated by the copending Application’s claims, they are also obvious in view of the copending Application’s claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. Claims 8-15 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8, 10, 9, and 12-16 respectively of copending Application No. 10/623,282 in view of Roberts U.S. Patent No. 5,541,654.

Regarding claim 8 of the instant Application, the claim 8 of the copending Application claims “an inspection device including at least a camera with the ability to selectively readout pixels of an imager of the camera”. However, the copending Application claim 8 does not explicitly claim a camera with the ability to selectively readout groups of pixels in one axis of an imager of the camera. Roberts teaches, in the same problem solving area of selective image accessing, a camera has ability to readout groups of pixels in one axis of an imager of the camera (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18;

Art Unit: 2624

“randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35).

Modifying the copending Application’s inspection system according to Roberts’s teachings would be able to provide a camera to readout groups of pixels in one axis of an imager of the camera. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (rectangular areas) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts’s teachings to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the “windows ... may be scanned at a frame rate much greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14) and therefore, it would have been obvious to one of the ordinary skill in the art to modify copending Application No. 10/623,282 according to Roberts.

Claims 8-19 are anticipated over claims 8, 10, 9, 12-20 respectively of copending Application No. 10/623,282.

This is a provisional obviousness-type double patenting rejection.

### ***Claim Objections***

4. Claims 5-7, 13-15, and 17-19 are objected to because of the following informalities:

Regarding claims 5 and 13, the limitation "...configured to program the camera ... based on a size of the semiconductor die or pattern." is objected because the claims **only claim** the semiconductor substrates comprise a plurality of semiconductor die. This results confusion when interpreting the claims because the claims never mentioned whether or not, the semiconductor substrate comprises a plurality of semiconductor pattern.

Referring to claims 17-19, the claims recall the size of the semiconductor die or pattern of the claim 16. However, claim 16 only discusses regarding to semiconductor die and not semiconductor pattern. Again, this results confusion when interpreting the claims because the claims never mention whether or not, the semiconductor die also is the semiconductor pattern.

Claims not specifically addressed are rejected because they are dependent of the rejected claims.

Appropriate correction is required.

The prior art rejection based on the Examiner's best understanding.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Roberts U.S. Patent No. 5,541,654.

Art Unit: 2624

Regarding claim 1, Robert teaches an inspection system including at least a camera with the ability to selectively readout (“The imaging device includes provision for random access of each image element or group of image elements in the array so that output signals indicative of all or of only selected parts of an imaged scene can be processed for the image information, if desired.”, abstract) readout a number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35).

For claim 2, Roberts further teaches a controller that programs the camera (imaging device that includes provision for random access of each image element or group of image elements, abstract) to readout a specified number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, lines 35-37).

Regarding claim 3, Roberts also teaches the camera includes an imager (imaging device) (column 4, line 19) having a first number of rows, and wherein the specified number of rows is less than the first number of rows (“randomly accessing the image elements individually or in the groups less than the full elements in the array”) (column 3, lines 35-37 and column 7, lines 39-45).

Regarding claim 8, Roberts teaches in inspection device including at least a camera with the ability to selectively readout (“The imaging device includes provision for random access of each image element or group of image elements in the array so that output signals indicative of

Art Unit: 2624

all or of only selected parts of an imaged scene can be processed for the image information, if desired.”, abstract) groups of pixels in one axis of an imager of the camera (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35).

Referring to claim 9, Robert teaches a controller (microprocessor) (FIG. 6, element 160) that programs (provides provision) (abstract, “The imaging device includes provision to random access ...”) the camera (imaging device) (abstract).

For claim 10, Robert also teaches the controller programs the camera (as discussed in claim 9) to readout a specified number of groups of pixels in one axis of the imager (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, lines 35-35).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-5, 8-13, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neumann U.S. Patent No. 6,693,664 and Roberts U.S. Patent No. 5,541,654.

Regarding claim 1, Neumann discloses an inspection system (abstract, first 5 lines) including a camera (electro-optical camera system with CCD matrix photo-detector at column 5,



Art Unit: 2624

lines 15-25) for taking an image of a semiconductor die, from which images of patterns of each dies (image of interest) (FIG. 1B, steps 6, 8 and 9) to readout a number of rows (“This optical configuration enables illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B).

Neumann does not teach a camera with the ability to selectively readout a number of rows (emphasis added).

Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability to selectively (“The imaging device includes provision for random access of each image element or group of image elements in the array so that output signals indicative of all or of only selected parts of an imaged scene can be processed for the image information, if desired.”, abstract) readout a number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35) of the image of interest (column 1, lines 20-23).

Modifying Neumann’s method of providing an inspection system according to Roberts would able to provide a camera that is selectively readout a number of rows at a region of interest. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (rectangular areas) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the “windows ... may be scanned at a frame rate much

greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.

For claim 2, Roberts further teaches a controller that programs the camera (imaging device that includes provision for random access of each image element or group of image elements, abstract) to readout a specified number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35).

Regarding claim 3, Roberts also teaches the camera includes an imager (imaging device) (column 4, line 19) having a first number of rows, and wherein the specified number of rows is less than the first number of rows (“randomly accessing the image elements individually or in the groups less than the full elements in the array”) (column 3, lines 35-37 and column 7, lines 39-45).

For claim 4, Neumann teaches the inspection system wherein the inspection system is configured to inspect semiconductor substrates (semiconductor wafer) (column 6, lines 3-7).

Regarding claim 5, Neumann teaches the inspection system (abstract, first 5 lines) wherein the semiconductor substrates (wafer) (FIG. 6 and FIG. 1A, step (1)) comprise a plurality of semiconductor die (wafer) (FIG. 6 and FIG. 1A, step (1)) and wherein the controller is configured (configuration) to program the camera (“This optical configuration enables

Art Unit: 2624

illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B) to readout semiconductor die/pattern (image of interest) (FIG. 1B, steps 6, 8 and 9).

Neumann does not teach a camera to read out the specified number of rows based on a size of semiconductor die/pattern (which can be an image of interest). Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability to readout the specified number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35) base on the image of interest (column 1, lines 20-23; FIG. 6, elements 172 and 174).

Modifying Neumann’s method of providing an inspection system according to Roberts would able to provide a camera that is readout a specified number of rows at a region of interest such as a semiconductor die/pattern. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (semiconductor die/pattern) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the “windows ... may be scanned at a frame rate much greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14)and

Art Unit: 2624

therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.

Regarding claim 8, Neumann discloses an inspection system (abstract, first 5 lines) including a camera (electro-optical camera system with CCD matrix photo-detector at column 5, lines 15-25) for taking an image of a semiconductor die, from which images of patterns of each dies (image of interest) (FIG. 1B, steps 6, 8 and 9) to readout groups of pixels (“This optical configuration enables illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B) in one axis of an imager (FIG. 2, element 12) of the camera (“electro-optical camera system” at column 5, line 17).

Neumann does not teach a camera with the ability to selectively readout groups of pixels (emphasis added).

Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability to selectively (“The imaging device includes provision for random access of each image element or group of image elements in the array so that output signals indicative of all or of only selected parts of an imaged scene can be processed for the image information, if desired.”, abstract) readout groups of pixels (“an imaging array” at column 3, line 14; “pixels” at column 3, line 22; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35) of the image of interest (column 1, lines 20-23).

Modifying Neumann's method of providing an inspection system according to Roberts would be able to provide a camera that is selectively readout groups of pixels at a region of interest. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (rectangular areas) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to "of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array", the "windows ... may be scanned at a frame rate much greater than would be possible if the entire array had to be scanned" (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.

Referring to claim 9, Robert teaches a controller (microprocessor) (FIG. 6, element 160) that programs (provides provision) (abstract, "The imaging device includes provision to random access ...") the camera (imaging device) (abstract).

For claim 10, Robert also teaches the controller programs the camera (as discussed in claim 9) to readout a specified number of groups of pixels in one axis of the imager ("an imaging array" at column 3, line 14; "windowing on the array" at column 3, line 18; "randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array" at column 3, line 35).

Regarding claim 11, Roberts also teaches an imager (imaging device) (column 4, line 19) having a first number of rows, each of the groups of pixels is a row of pixels, and the specified

Art Unit: 2624

number of groups of pixels is less than the first number of rows (“randomly accessing the image elements individually or in the groups less than the full elements in the array”) (column 3, lines 35-37 and column 7, lines 39-45).

For claim 12, Neumann teaches the inspection system wherein the inspection system is configured to inspect semiconductor substrates (semiconductor wafer) (column 6, lines 3-7).

Regarding claim 13, Neumann teaches the inspection system (abstract, first 5 lines) wherein the semiconductor substrates (wafer) (FIG. 6 and FIG. 1A, step (1)) comprise a plurality of semiconductor die (wafer) (FIG. 6 and FIG. 1A, step (1)) and wherein the controller is configured (configuration) to program the camera (“This optical configuration enables illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B) to readout semiconductor die/pattern (image of interest) (FIG. 1B, steps 6, 8 and 9).

Neumann does not teach a camera to read out the specified number of groups of pixels based on a size of semiconductor die/pattern (which can be image of interest). Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability to readout the specified number of groups of pixels (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35) base on the image of interest (column 1, lines 20-23; FIG. 6, elements 172 and 174).

Modifying Neumann’s method of providing an inspection system according to Roberts would able to provide a camera that is readout a specified number of groups of pixels at a region

Art Unit: 2624

of interest such as a semiconductor die/pattern. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (semiconductor die/pattern) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the “windows ... may be scanned at a frame rate much greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.

Regarding claim 16, Neumann teaches an automated method (column 7, lines 13-16) for inspecting (abstract, first 5 lines) a plurality of semiconductor die (FIG. 1A, step (1)), the method comprising:

Providing a camera including an imager (electro-optical camera system with CCD matrix photo-detector to take image at column 5, lines 15-25);

Capturing image frames (column 5, lines 60-65) of the plurality of semiconductor die with the imager (wafer of semiconductor dies) (FIG. 1A, step (1)), each captured frame including first number of rows of pixels (“This optical configuration enables illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B);

Reading out pixel data from the imager for each captured frame (FIG. 1B, step (8) and step (8), (A));

Identifying defects in the plurality of semiconductor die based on the pixel data read out of the imager (FIG. 1B, step (8), (B)).

Neumann does not explicitly teaches a camera wherein each captured frame including a second number of rows of pixels that is less than the first number of rows of pixels.

Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability readout a second number of rows (“windowing on the array” at column 3, line 18 of the image of interest at column 1, lines 20-23) that is less than the first number of rows of pixels (“randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, lines 35-37; full elements of array is first number of rows).

Modifying Neumann’s method of providing an inspection system according to Roberts would able to provide a camera that is selectively readout a number of rows at a region of interest. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those image of interest (rectangular areas) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the “windows ... may be scanned at a frame rate much greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.



Regarding claim 17, Neumann teaches the inspection system (abstract, first 5 lines) wherein the semiconductor substrates (wafer) (FIG. 6 and FIG. 1A, step (1)) comprise a plurality of semiconductor die (wafer) (FIG. 6 and FIG. 1A, step (1)) and wherein the controller is configured (configuration) to program the camera (“This optical configuration enables illumination of a wafer die with a single laser pulse and simultaneous imaging by an array, of twenty-four two dimensional CCD matrix photo-detectors, having a total of about 48 million (48 mega) pixels” at column 11, lines 2-6 and FIG. 5B) to readout semiconductor die/pattern (image of interest) (FIG. 1B, steps 6, 8 and 9).

Neumann does not teach a camera to read out the specified number of rows based on a size of semiconductor die/pattern (which can be an image of interest). Roberts teaches, in the same problem solving area of selective image accessing, a camera with the ability to readout the specified number of rows (“an imaging array” at column 3, line 14; “windowing on the array” at column 3, line 18; “randomly accessing the image elements individually or in groups of less than the full plurality of elements on the array” at column 3, line 35) base on the image of interest (column 1, lines 20-23; FIG. 6, elements 172 and 174).

Modifying Neumann’s method of providing an inspection system according to Roberts would able to provide a camera that is readout a specified number of rows at a region of interest such as a semiconductor die/pattern. This would improve processing because rather than capturing the entire image, according to the teaching of Roberts, only those images of interest (semiconductor die/pattern) need to be scanned out of the imaging device to begin with. One would be motivated to modify Neumann according to Roberts to “of the reduced number of pixels in the windows ... in comparison to the number of pixels in the entire array”, the

Art Unit: 2624

“windows ... may be scanned at a frame rate much greater than would be possible if the entire array 12 had to be scanned” (Roberts, column 10, lines 15-20), thus speed up the processing, reduce the buffer (column 9, line 35-36) and minimizes the chances of the imaging device being overload with incoming light so that the imaging system is blinded (column 11, lines 10-14) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Roberts.

9. Claims 6, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Neumann U.S. Patent No. 6,693,664 and Roberts U.S. Patent No. 5,541,654, as discussed in claim 5, and further in view of Tsuneta et al. U.S. Patent No. 6,570,156.

Regarding claim 6, Neumann teaches the adjustments of focus for field of view of the camera to properly position (fit) to the semiconductor die. Neumann does not explicitly teach that the size of the semiconductor is less than field of view of the camera. Tsuneta teaches a semiconductor inspection system (FIG. 10, “select inspected filed” and “inspect”; and column 26, line 55) wherein the size of the semiconductor die/pattern is less than field of view of the camera (when the field of view of the camera is clipped, thus the semiconductor pattern is smaller) (column 26, lines 65-67).

Modifying Neumann’s method of inspecting semiconductor substrate according to Tsuneta would be able to clip the field of view to the size of the semiconductor pattern. This would improve processing because according to Tsuneta, “the same size of image will be suitable for the registered image to be compared with”, so that the “position of clipped field of view will be shifted to the next to iteratively evaluate the consistency of the pattern” (column 26, line 65 to

Art Unit: 2624

column 27, lines 7) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Tsuneta.

For claim 14, please refer back to the teachings and explanations of claim 6.

For claim 18, please refer back to the teachings and explanations of claim 6.

10. Claims 7, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Neumann U.S. Patent No. 6,693,664 and Roberts U.S. Patent No. 5,541,654, as discussed in claim 5, and further in view of Isogai et al. U.S. Patent No. 6,457,232.

Regarding claim 7, Neumann teaches the adjustments of focus for field of view of the camera to properly position (fit) to the semiconductor die. Neumann does not explicitly teach that the size of the semiconductor is greater than field of view of the camera. Isogai teaches a chip substrate inspection method (column 2, lines 31-49) wherein the chip pattern is greater than a field of view of the camera (column 25, lines 13-22).

Modifying Neumann's method of inspecting semiconductor substrate according to Isogai would be able to determine the die or pattern that is greater than field of view of the camera (column 25, lines 19-25). This would improve processing because according to Isogai, by determining the die/pattern that is greater than field of view of the camera would allow the system to take a different image that is substantially identical with the die/pattern/icon (column 25, lines 20-34) to further determine the standard chip with accuracy (column 2, lines 40-49) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Neumann according to Isogai.

For claim 15, please refer back to the teachings and explanations of claim 6.

For claim 19, please refer back to the teachings and explanations of claim 6.

## ***CONCLUSION***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor/chip/wafer inspection and camera system:

U.S. Pat. No. 6,801,650 to Kikuchi et al., teaches method for controlling focal point position of UV light for inspection.

U.S. Pat. No. Nakamura et al. to Nakamura et al., teaches method comprising photosensor system and drive control.

U.S. Pat. No. 5,621,811 to Roder et al., teaches learning method for detecting and controlling solder defects.

U.S. Pat. No. 6,936,835 to Nishiyama et al., teaches method for inspecting particles or defects of a semiconductor device.

U.S. Pat. No. 6,522,777 to Paulsen et al., teaches combined 3D and 2D-scanning machine vision system for inspection.

U.S. Pat. No. 4,668,982 to Tinnerino, teaches misregistration/distortion correction scheme.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Q. Le whose telephone number is 571-272-7424. The examiner can normally be reached on 8:30 A.M - 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on 571-272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian Le  
September 9, 2006